

impurity is doped from a surface of the epitaxial film by a vapor phase diffusion method to form an impurity doped region in the epitaxial film. The final step is such that the epitaxial film having no impurity doped or a low concentration impurity doped in the epitaxial film is formed to fill an inside of the trench. The low concentration impurity of the epitaxial film in the final step has an impurity concentration lower than that in the first step. In this case, the epitaxial film is filled in the trench with void-less structure, and further, the impurity in the epitaxial film can be formed uniformly.

[0014] Preferably, the step of forming the epitaxial film further includes a vapor phase diffusion step. The vapor phase diffusion step is such that an impurity is doped from the bottom and the sidewall of the trench by a vapor phase diffusion method to form an impurity doped region in the bottom and the sidewall of the trench. The final step is such that the epitaxial film having no impurity doped or a low concentration impurity doped in the epitaxial film is formed to fill an inside of the trench. The low concentration impurity of the epitaxial film in the final step has an impurity concentration lower than that in the impurity doped region of the bottom and the sidewall of the trench. In this case, the epitaxial film is filled in the trench with void-less structure, and further, the impurity in the epitaxial film can be formed uniformly.

[0015] Preferably, the step of forming the epitaxial film further includes a first step. The first step is such that the epitaxial film having no impurity doped or an impurity doped in the epitaxial film is formed on the bottom and the sidewall of the trench to have a predetermined thickness. The final step is such that the epitaxial film having a high concentration impurity doped in the epitaxial film is formed to fill an inside of the trench. The high concentration impurity of the epitaxial film in the final step has an impurity concentration higher than that in the first step. The final step is performed under a predetermine vacuum pressure lower than that of the first step. In this case, the epitaxial film is filled in the trench with void-less structure, and further, the impurity in the epitaxial film can be formed uniformly.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description made with reference to the accompanying drawings. In the drawings:

[0017] FIG. 1 is a cross sectional view showing a vertical trench gate MOSFET according to a first embodiment of the present invention;

[0018] FIG. 2 is a partially enlarged cross sectional view showing a device portion of the MOSFET according to the first embodiment;

[0019] FIGS. 3A to 3D are cross sectional views explaining a method for manufacturing the MOSFET according to the first embodiment;

[0020] FIGS. 4A to 4D are cross sectional views explaining the method for manufacturing the MOSFET according to the first embodiment;

[0021] FIGS. 5A to 5C are partially enlarged cross sectional views explaining the method for manufacturing the MOSFET according to the first embodiment;

[0022] FIG. 6 is a graph explaining a relationship between a growth rate ratio and a process temperature with and without HCl gas, according to the first embodiment;

[0023] FIG. 7 is a graph explaining a relationship between a growth rate and a process temperature with using different gases, according to the first embodiment;

[0024] FIG. 8 is a graph explaining a normalized ON-state resistance and a breakdown voltage in different devices, according to the first embodiment;

[0025] FIG. 9A is a photograph of cross sectional SEM image showing a trench in a silicon substrate as a comparison of the first embodiment, and FIG. 9B is an illustrative view of photograph in FIG. 9A;

[0026] FIG. 10A is a photograph of cross sectional SEM image showing a silicon substrate after a 3  $\mu\text{m}$ -deposition with using a dichlorosilane gas at a temperature higher than 1100° C., and FIG. 10B is an illustrative view of photograph in FIG. 10A;

[0027] FIG. 11A is a photograph of cross sectional SEM image showing a silicon substrate after a 3  $\mu\text{m}$ -deposition with using a mixed gas at a temperature higher than 1100° C., and FIG. 11B is an illustrative view of photograph in FIG. 11A;

[0028] FIG. 12A is a photograph of cross sectional SEM image showing a silicon substrate after a 3  $\mu\text{m}$ -deposition with using a dichlorosilane gas at a temperature equal to or lower than 1100° C., and FIG. 12B is an illustrative view of photograph in FIG. 12A;

[0029] FIG. 13A is a photograph of cross sectional SEM image showing a silicon substrate after a 3  $\mu\text{m}$ -deposition with using a mixed gas at a temperature equal to or lower than 1100° C., and FIG. 13B is an illustrative view of photograph in FIG. 13A;

[0030] FIG. 14A is a photograph of cross sectional SEM image showing a silicon substrate after a 10  $\mu\text{m}$ -deposition with using a mixed gas at a temperature equal to or lower than 1100° C., and FIG. 14B is an illustrative view of photograph in FIG. 14A;

[0031] FIGS. 15A to 15D are cross sectional views explaining a method for manufacturing a semiconductor substrate according to a second embodiment of the present invention;

[0032] FIGS. 16A to 16D are cross sectional views explaining a method for manufacturing a semiconductor substrate according to a third embodiment of the present invention;

[0033] FIGS. 17A to 17D are timing charts showing process conditions of the manufacturing method in each process, according to the third embodiment;

[0034] FIGS. 18A to 18E are cross sectional views explaining a method for manufacturing a semiconductor substrate according to a fourth embodiment of the present invention;

[0035] FIGS. 19A to 19D are timing charts showing process conditions of the manufacturing method in each process, according to the fourth embodiment;